

NCT3612Y

High Integrated 3-Phase Gate Driver

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1. GENERAL DESCRIPTION

The NCT3612Y is a monolithic half-bridge gate drive IC, it is designed for BLDC motor driver applications, which operate up to 35V. Integrated 3-channel N-MOSFET driver for 3-phase BLDC with channel direction control by unique DIR pin. The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage. It also build-in bootstrap diodes that can reduce output component. NCT3612 offers an extremely compact high performance half-bridge inverter in a small QFN28 4*4 package for two or three-phase motor driver.

2. FEATURES

- 6 ~ 35V Operate Supply Voltage Range
- 250mA Source & 500mA Sink Gate Drive Current Capability @VCC > 15V
- Integrated 2 LDO
- 5V LDO Output for MCU power supply
- 12V LDO for internal use
- Sleep Mode Support (< 100uA)
- Integrated bootstrap diode
- Direction Control for Motor Forward / Reverse sequence by PWM input signal
- Protection:
 - UVLO (Under Voltage Lockout)
 - Thermal Shutdown Protection (@165°C)

3. APPLICATIONS

- Power Tool
- BLDC Motor
- Electronic Speed Controller unit (ESC)
- Robotics & RC Servo

4. PIN INFORMATION

4.1 Pin Configuration

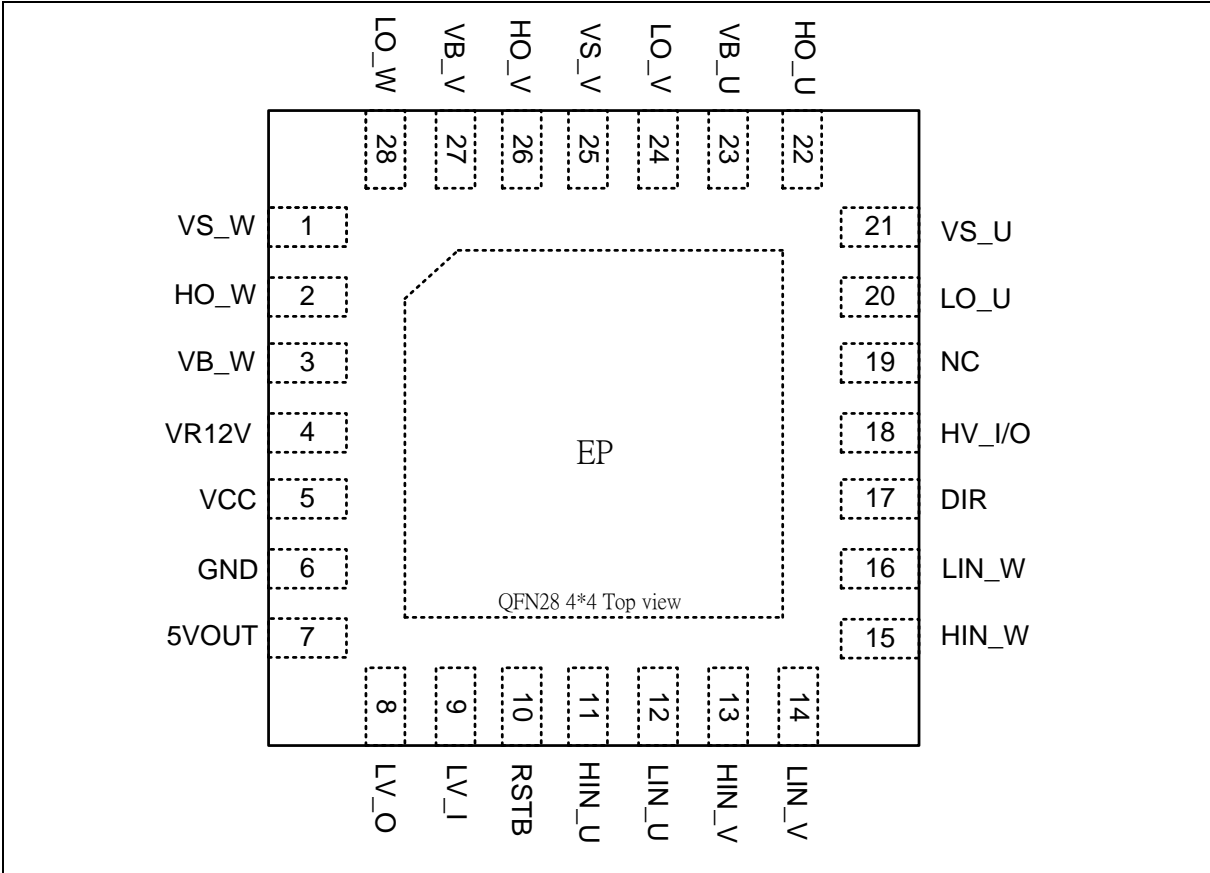


Figure 4-1 NCT3612Y QFN 28-pin Diagram

4.2 Pin Description

PIN	PIN NAME	FUNCTION
1.	VS_W	W-Phase high-side floating supply offset voltage.
2	HO_W	W-phase high-side floating output voltage.
3	VB_W	W-phase high-side floating supply absolute voltage.
4	VR12V	Linear regulator output and gate driver supply voltage
5	VCC	Power supply voltage.
6	GND	Ground.
7	5VOUT	Internal 5V LDO Reference out.
8	LV_O	Low voltage signal Output. This is the low voltage inverter output of HV_I/O.
9	LV_I	Low voltage signal Input. Connect an input signal. As the signal is high level (>2.4V) and it will pull the HV_I/O down to GND. As the signal is low level (<0.8V) and it will make the HV_I/O pull up to external voltage.
10	RSTB	Open Drain output with 2uA pull up. If this pin is low, then NCT3612Y enter sleep mode.
11	HIN_U	Signal input high active for high side. It controls the upper MOSFET of U phase. It will turn on the MOSFET when this pin is high, and turn off the MOSFET when this pin is low. The pin integrated internal pull-down resistor to prevent fault turns on.
12	LIN_U	Signal input high active for Low side. It controls the upper MOSFET of U phase. It will turn on the MOSFET when this pin is high, and turn off the MOSFET when this pin is low. The pin integrated internal pull-down resistor to prevent fault turns on.
13	HIN_V	Signal input high active for high side. It controls the upper MOSFET of V phase. It will turn on the MOSFET when this pin is high, and turn off the MOSFET when this pin is low. The pin integrated internal pull-down resistor to prevent fault turns on.
14	LIN_V	Signal input high active for Low side. It controls the upper MOSFET of V phase. It will turn on the MOSFET when this pin is high, and turn off the MOSFET when this pin is low. The pin integrated internal pull-down resistor to prevent fault turns on.
15	HIN_W	Signal input high active for high side. It controls the upper MOSFET of W phase. It will turn on the MOSFET when this pin is high, and turn off the MOSFET when this pin is low. The pin integrated internal pull-down resistor to prevent fault turns on.
16	LIN_W	Signal input high active for Low side. It controls the upper MOSFET of W phase. It will turn on the MOSFET when this pin is high, and turn off the MOSFET when this pin is low. The pin integrated internal pull-down resistor to prevent fault turns on.
17	DIR	Direction Control (PWM output sequence) Signal input for Pin11~16 Sequence This pin default is pull up to 5V PWM sequence = U,V,W if DIR=5V PWM sequence = W,V,U if DIR = GND
18	HV_I/O	High voltage signal input/output. This pin can be input or output. As it be input, it should be connected with a high voltage (>5V) signal. As it be output, it will be the high voltage inverter output of LV_I.
19	NC	
20	LO_U	U-phase low-side output voltage.

21	VS_U	U-Phase high-side floating supply offset voltage.
22	HO_U	U-phase high-side floating output voltage.
23	VB_U	U-phase high-side floating supply absolute voltage.
24	LO_V	V-phase low-side output voltage.
25	VS_V	V-Phase high-side floating supply offset voltage.
26	HO_V	V-phase high-side floating output voltage.
27	VB_V	V-phase high-side floating supply absolute voltage.
28	LO_W	W-phase low-side output voltage.

5. BLOCK DIAGRAM

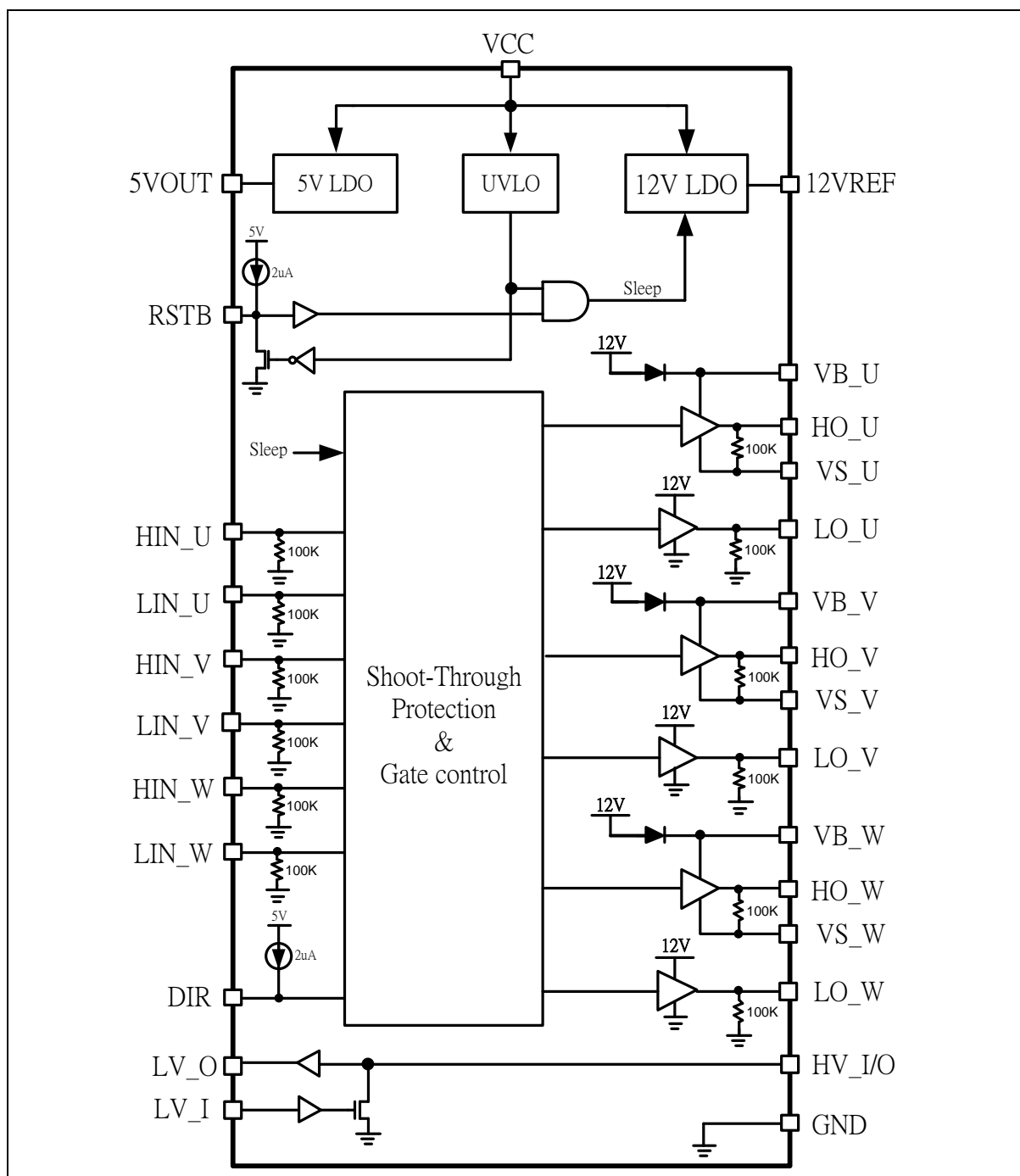


Figure 5-1 NCT3612Y Block Diagram

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
VCC	Input supply voltage.	-0.3 to 40	V
VR12V	Linear regulator output and gate driver supply voltage.	-0.3 to 15	V
VB	High-side floating supply absolute voltage.	-0.3 to VS+VR12V	V
VS	High-side floating supply offset voltage.	-2 to VCC+2	V
HO	High-side floating output voltage.	VS-0.3 to VB+0.3	V
LO	Low-side output voltage.	-0.3 to VR12V+0.3	V
Other pins	5VOUT, LV_O, LV_I, RSTB, HIN, LIN, DIR.	-0.3 to 6	V
θ_{JA}	Thermal Resistance,	40	°C/W
θ_{JC}	Thermal Resistance,	10	°C/W
θ_{STG}	Storage Temperature	-50 to 150	°C
θ_J	Junction Temperature	150	°C
ESD Rating	Human Body Mode(all pins)	± 2	KV
	Charge Device Mode	± 500	V
	Latch-up	± 100	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 Recommended Operating Conditions

PARAMETER	RATING	UNIT
VCC supply voltage	6 to 35	V
5VLDO supply Output Current	35	mA
Operating temperature	-40 to 105	°C
Junction temperature	-40 to 125	°C

Note: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

6.3 DC Electrical Characteristics

(VCC= 35V, TA = TJ = 25° C, unless otherwise specified)

Parameter	Symbol	Test condition		Min.	Typ.	Max.	Unit
Supply voltage							
Input supply voltage	VCC			6	---	35	V
VCC UVLO turn-on threshold	UVLO+			3.5	4	4.5	V
VCC UVLO turn-off threshold	UVLO-	VCC Falling		3.1	3.6	4.1	V
VCC UVLO threshold hysteresis				---	0.4	---	V
VCC operation current		PWM =20KHz, Duty=50%		---	20	---	mA
VCC sleep mode current		RSTB=Low		---	100	---	uA
Gate Driver Output							
Sourcing peak current	Io+	CL=0.22uF, PWM =1KHz, Duty=50%	VIN≥15V, TA = 25° C	160	250	---	mA
			VIN≥15V, Full Temperature	145	---	---	mA
			VIN=7V, TA = 25° C	40	75	---	mA
			VIN=7V, Full Temperature	30	---	---	mA
Sinking peak current	Io-	CL=0.22uF, PWM =1KHz, Duty=50%	VIN≥15V, TA = 25° C	330	500	---	mA
			VIN≥15V, Full Temperature	290	---	---	mA
			VIN=7V, TA = 25° C	75	150	---	mA
			VIN=7V, Full Temperature	55	---	---	mA
Turn-on propagation delay	ton	CL=1nF		---	50	---	nS
Turn-off propagation delay	toff	CL=1nF		---	50	---	nS
Turn-on rise time	tr	CL=1nF		---	50	---	nS
Turn-off fall time	tf	CL=1nF		---	30	---	nS
PWM delay matching	MT			---	50	---	nS
Pull low resistance	Ro			---	100	---	KΩ
Logic Input							
Voltage high Level	VIH			2.0	---	---	V
Voltage low Level	VIL			---	---	0.8	V
HIN/LIN pull low Resistance	RI			---	100	---	KΩ
Internal 5V/12V regulator							
5V output voltage	5VOUT			4.75	5	5.25	V
5V output current Limit	5VIOUT	VCC=35 , TA = 25° C		---	35	---	mA

12V output voltage	V _{R12V}	RSTB=High		11	12	13	V
12V output current Limit	12V _{IOUT}	VCC=35 , TA = 25° C		---	35	---	mA
VB_U/V/W voltageg	VB	C _{BS} =1uF	VIN≥15V, TA = 25° C	9.5	10.5	---	V
			VIN≥15V, Full Temperature	9	---	---	V
			VIN=7V, TA = 25° C	4.5	5.5	---	V
			VIN=7V, Full Temperature	4	---	---	V
Thermal Protection							
Thermal shutdown temperature	T _{SD}			---	165	---	℃
Thermal shutdown hysteresis	T _{SDHYS}			---	50	---	℃

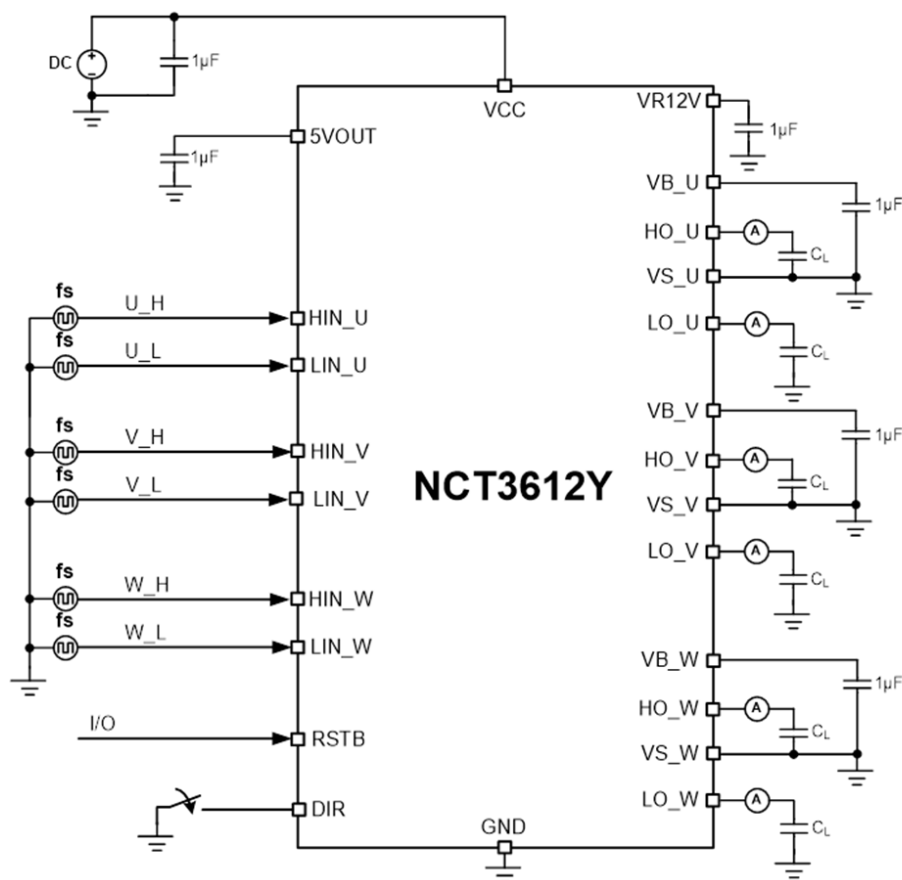


Figure 6.3-1 DC Electrical Characteristics Test Circuit

6.4 Timing Diagram

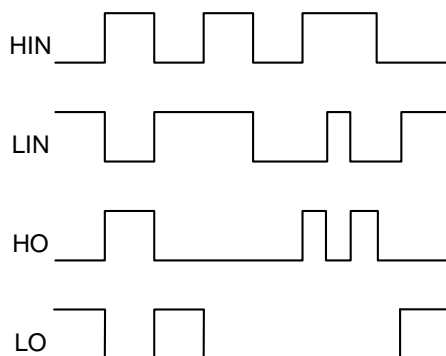


Figure 6.4-1 Input / Output Timing Diagram

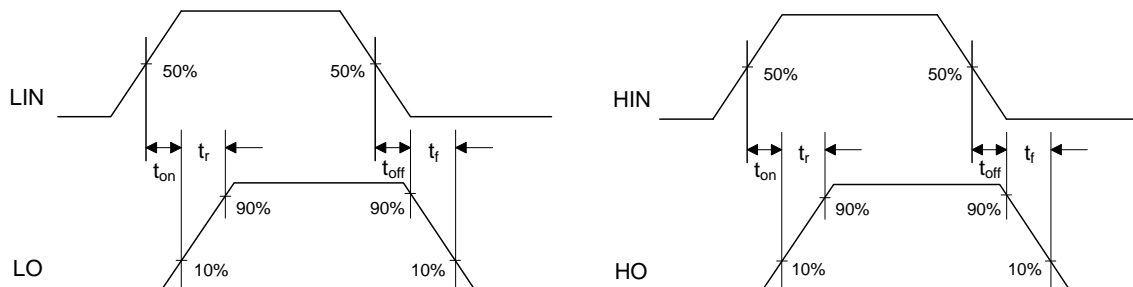


Figure 6.4-2 Switching Time Waveform Definition

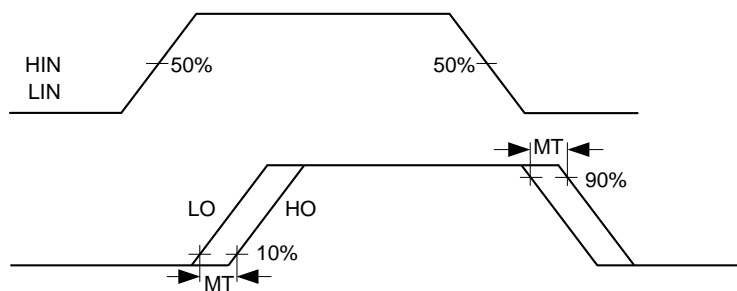


Figure 6.4-3 Delay Matching Waveform Definition

7. TYPICAL CHARACTERISTIC

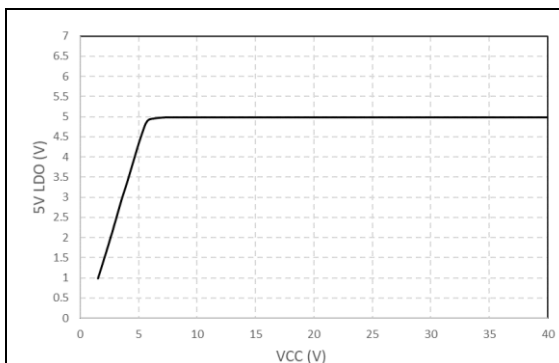


Figure 7-1 VCC vs. 5V LDO Voltage

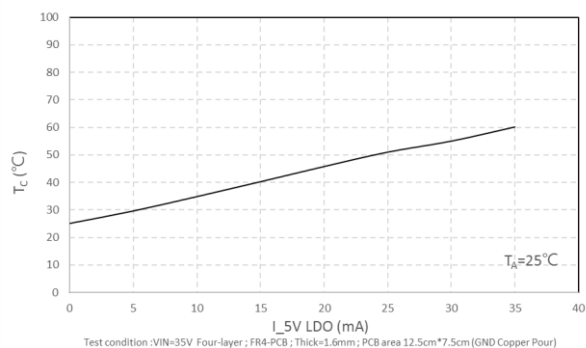


Figure 7-2 5V LDO Current vs. IC temperature

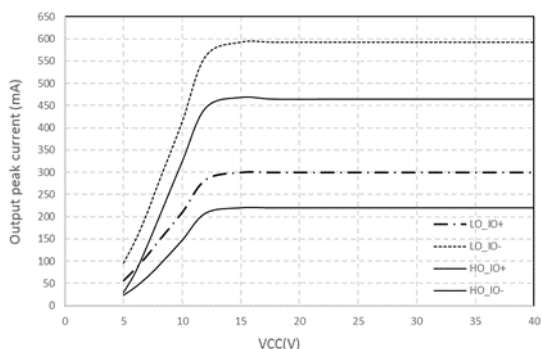


Figure 7-3 VCC vs. Output peak current

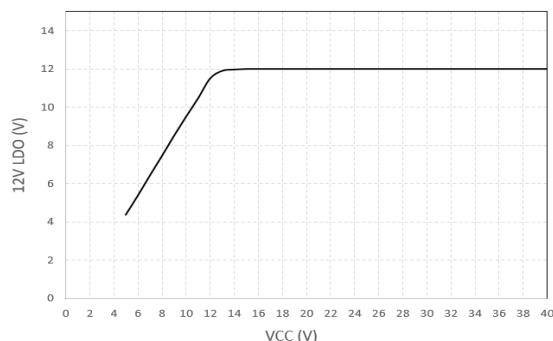


Figure 7-4 VCC vs. 12V LDO Voltage

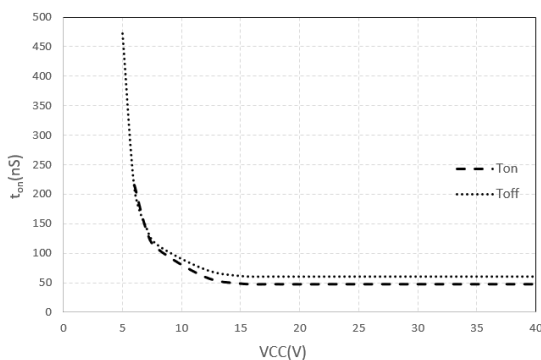


Figure 7-5 VCC vs. Ton/Toff propagation delay

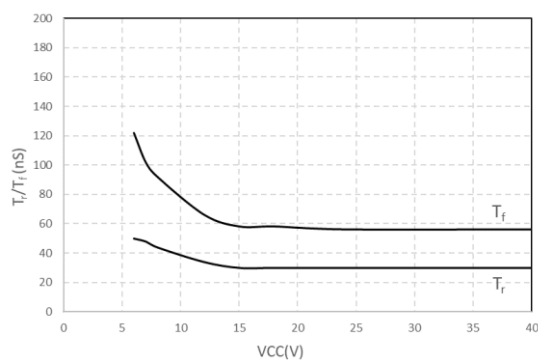


Figure 7-6 VCC vs. Turn-on/off rise time

8. TYPICAL APPLICATION CIRCUIT

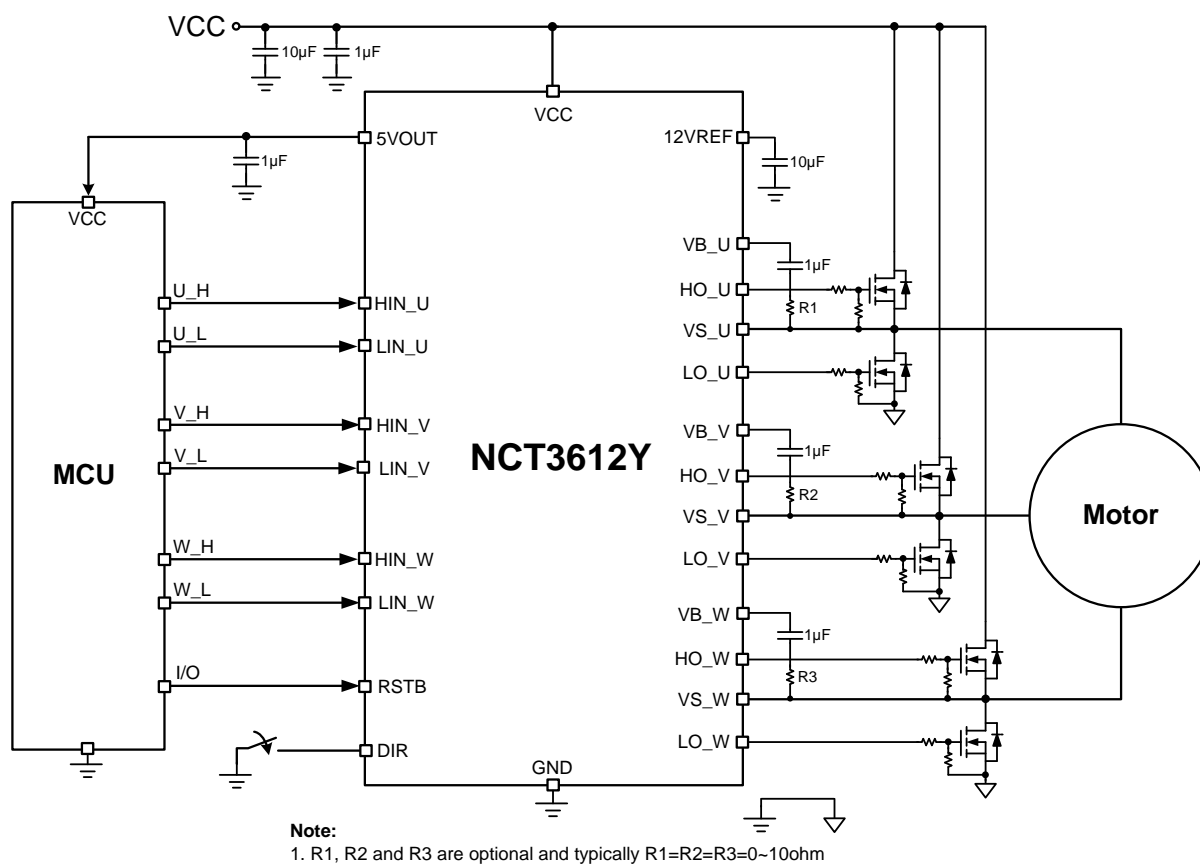


Figure 8-1 NCT3612Y Typical Application Circuit

9. FUNCTIONAL DESCRIPTION

9.1 Sleep Mode

The NCT3612Y provides a sleep mode for power saving. RSTB pin is Open Drain output 2uA pull up. And if this pin is low, then NCT3612Y enter sleep mode & standby current < 100uA. In sleep mode, NCT3612Y will disable 12VLDO and shut all driver output off. It means HO_U/V/W and LO_U/V/W will at low level no matter HIN_U/V/W and LIN_U /V/W signal. This pin can also be controlled by MCU I/O pad.

9.2 UVLO (Under Voltage LockOut)

The NCT3612Y incorporates an under voltage lockout circuit to disable the device when the input supply voltage is insufficient. During power up, internal circuits are held inactive until input supply voltage exceeds the UVLO threshold voltage of 4.5V. Once the UVLO rising threshold is reached, internal circuitry will immediately enable. It also builds-in the hysteresis of 0.4V when input supply voltage below 4.1V the NCT3612Y will immediately be disabled.

9.3 Internal Regulator

The NCT3612 includes a 5V LDO and a 12V LDO. Both 5V and 12V output current capacity are up to 30mA. Suggest connect a 10uF capacitor from LDO output to GND.

9.4 PWM Sequence Direction Control

The NCT3612Y support PWM sequence direction control. PWM0~5 input can be reordering the sequence by Pin DIR control. There is built-in pull-up resistor in pin DIR.

PWM sequence = PWM0~5 if DIR=5V

PWM sequence = PWM5~0 if DIR = GND

9.5 HV_I/O

The HV_I/O is as Fig1. HV_I/O pin could be high voltage input or output. As HV_I/O is high voltage input, the LV_O will be non-inverter low voltage output. As HV_I/O is high voltage output, it would be an open drain output that is pulled up to external voltage through a resister. Connect a low voltage input signal and it will produce an inverter high voltage on HV_I/O pin.

For example:

If 5V signal input on LV_I and the HV_I/O will be 0V.

If 0V signal input on LV_I and the HV_I/O will be pull up to external voltage (Fig7 shows 12V).

If 12V signal input on HV_I/O and the LV_O will be 5V.

If 0V signal input on HV_I/O and the LV_O will be 0V.

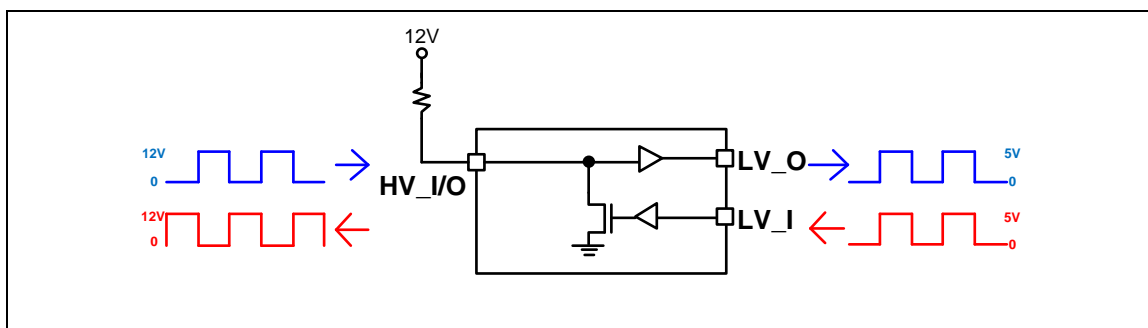


Figure 9-1 The Function Block of HV_I/O, LV_O and LV_I

9.6 Thermal Shutdown

The NCT3612Y has a thermal shutdown circuitry to limit the junction temperature. When the junction temperature exceeds 165° C, the thermal shutdown circuits disable the output, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 50° C, resulting in a pulsed output during continuous thermal overload conditions. The thermal protection is designed to protect the IC in the event of over temperature conditions. For reliable operation, the junction temperature cannot exceed 125° C.

9.7 Logic Functions

Input		Output	
HIN_U/V/W	LIN_U/V/W	HO_U/V/W	LO_U/V/W
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

9.8 Short-pulse Width

NCT3612Y will start to generate output as input PWM signal voltage > input threshold (VIH). Even the input signal pulse width t is very short, NCT3612Y will also generate output.

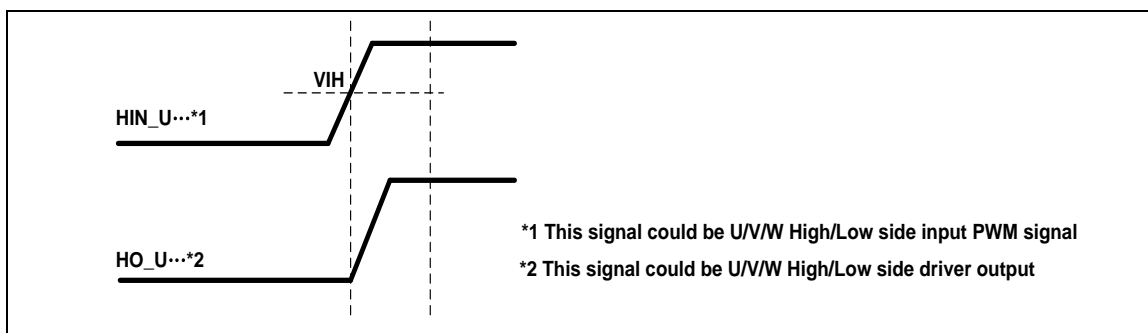


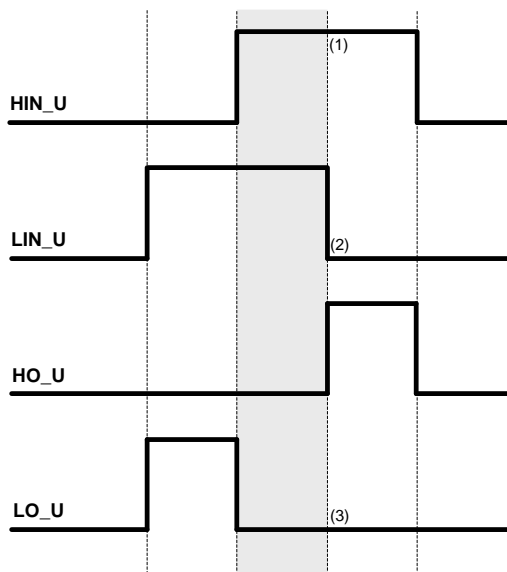
Figure 9-2 The Output start generation

9.9 Shoot-through Protection Functions

The NCT3612Y includes non-overlapping function, which prevents the high-side and low-side FETs from conducting at the same time. When switching FETs on, this handshaking prevents the high or low-side FET from turning on until the opposite FET has been turned off.

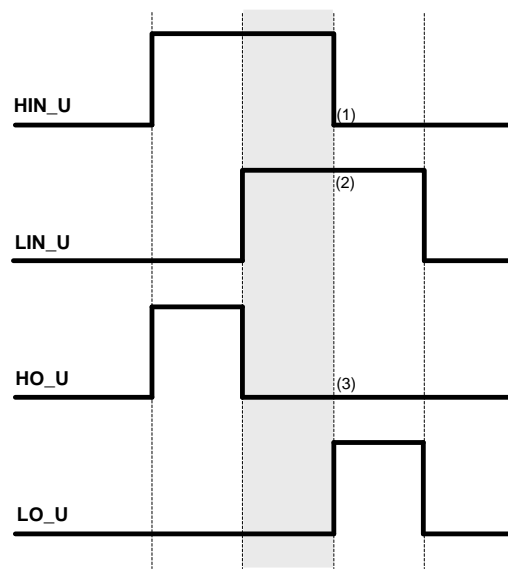
The non-overlapping function works as below:

As “HIN_U” input signal is high and “LIN_U” input signal is low, the “HO_U” will go high if “LO_U” reach a predetermined low level (ex:Fig9). Base the same way, the “LO_U” will go high as “HIN_U” input signal is low, “LIN_U” input signal is high and the difference of “HO_U” reach a predetermined low level (ex:Fig10). Base on this action, it can actually prevent the high side and low side FETs from conducting at the same time. The Phase V and W work by the same way.



HO_U goes high because
 (1) HIN_U is high &
 (2) LIN_U is low &
 (3) LO_U reach a predetermined low level

Figure 9-3 The HO Rise



LO_U goes high because
 (1) HIN_U is low &
 (2) LIN_U is high &
 (3) HO_U reach a predetermined low level

Figure 9-4 The LO Rise

10. APPLICATION INFORMATION

10.1 Bootstrap Capacitor Selection

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. The bootstrap capacitor (CBOOT) is charged by VCC through the internal diode when low side MOSFET Q2 turns on and high side MOSFET Q1 turns off. It provides high side MOSFET Q1 driving voltage when high side MOSFET Q1 turns on and low side MOSFET Q2 turns off.

An easy way to determine the CBOOT is the following equation:

$$C_{BOOT} \geq 10C_{GATE \text{ of Upper N-MOSFET}}$$

In most application, we suggest 0.1uF to 1uF MLCC for a general CBOOT value. To remind that a large CBOOT value causes more power dissipation when charging the CBOOT.

10.2 VR12V Capacitor Selection

Selecting VR12V capacitor is also need to be noticed. Due to bootstrap capacitor (CBOOT) is charged by VR12V so we have to provide an enough VR12V to charge it. An easy way to determine the CLDO12V is the following equation:

$$C_{VR12V} \geq 10C_{BOOT}$$

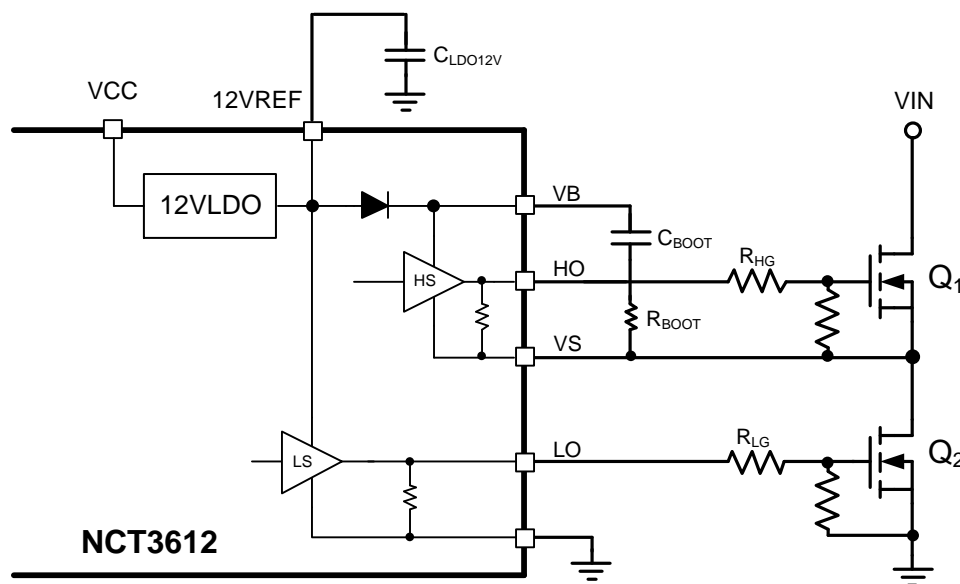


Figure 10-1 Bootstrap Circuit

10.3 High Side MOSFET Maximum On Time Limitation

This bootstrap power supply technique has the advantage of being simple and low cost. However, it has some limitations, on time of duty-cycle is limited by the requirement to refresh the charge in the bootstrap capacitor.

In NCT3612 include internal level shifter circuit is for high side gate driver. It is supplied by "VB-VS" voltage. It means we have to note the "VB-VS" voltage should not below internal level shifter required minimum voltage during CBOOT discharge (high side MOSFET turns on and low side MOSFET turns off).

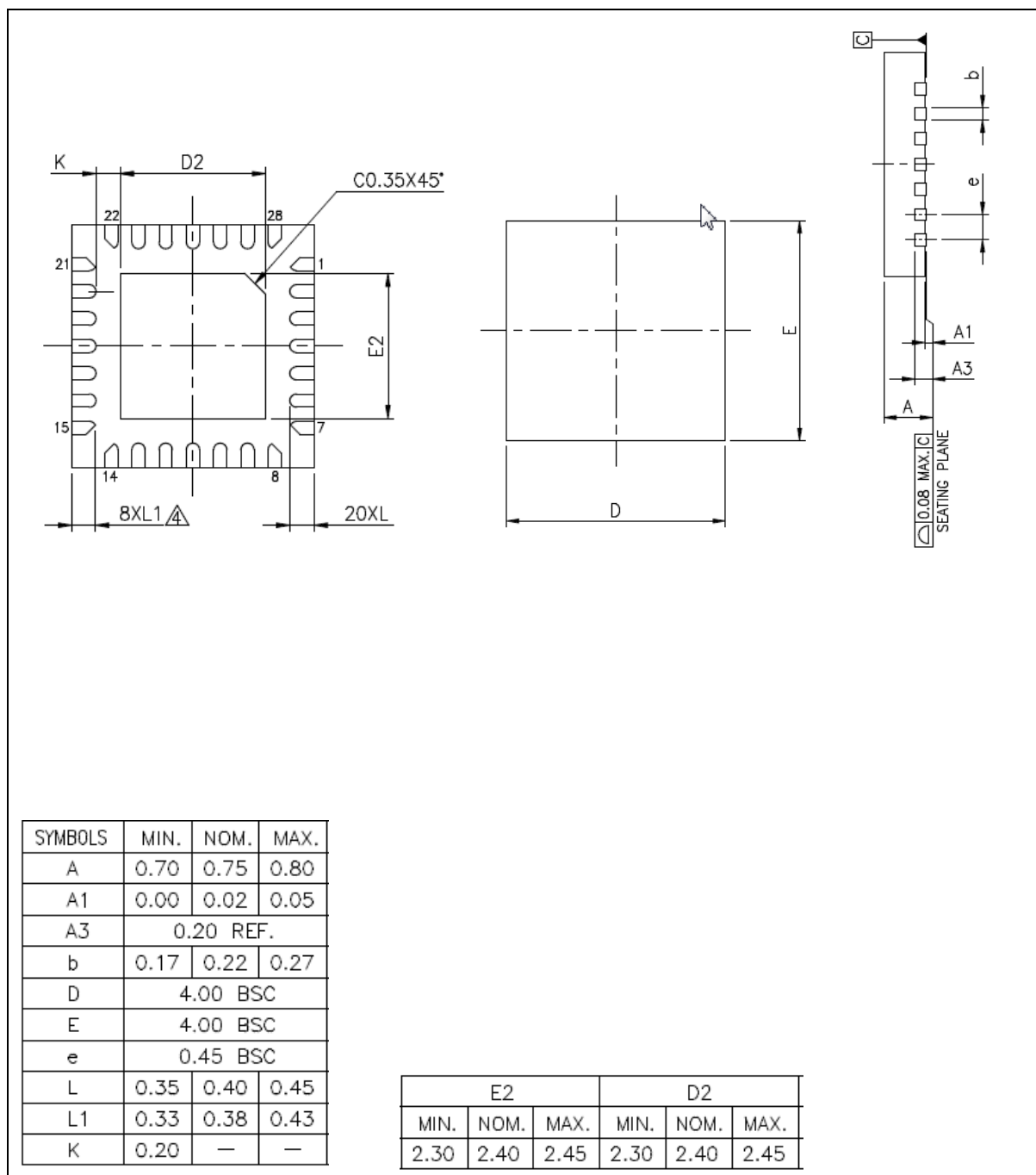
It is also means the maximum (high side) on time is limited. We suggest maximum on time do not exceed 50uS at CBOOT=0.1uF and 500uS at CBOOT=1uF.

10.4 External MOSFET Slew Rate Control

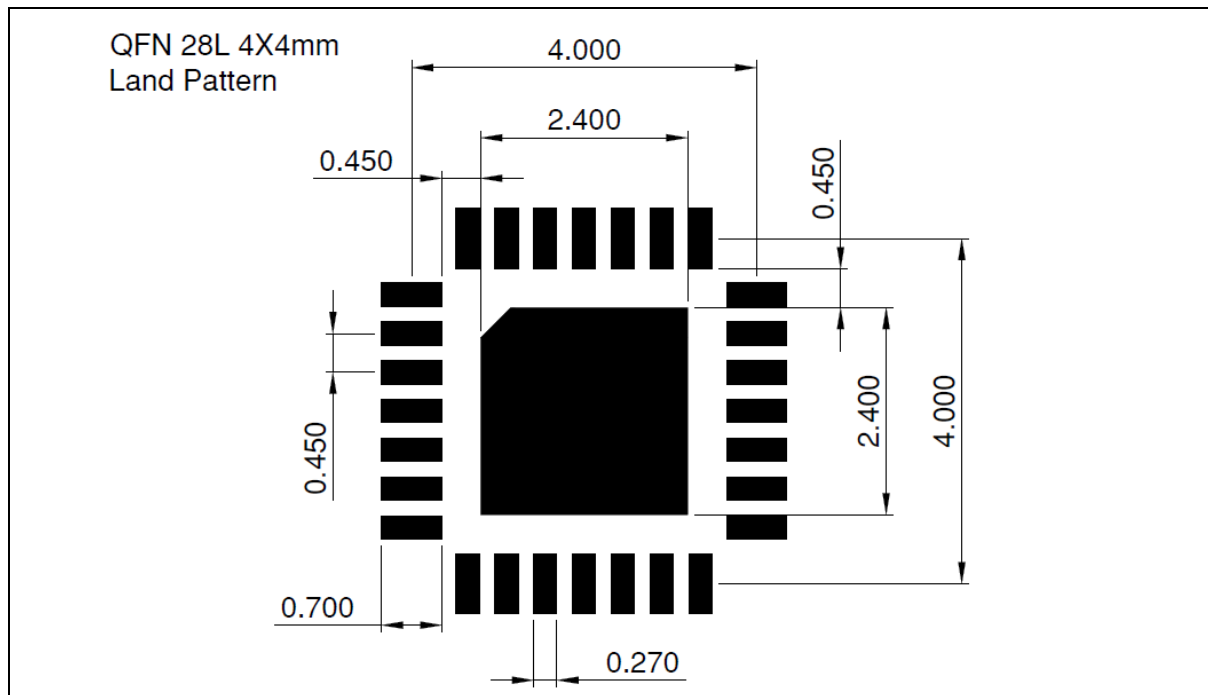
The Q1 gate resistor (RHG) and Q2 gate resistor (RLG) are slew rate control for switching upper N-MOSFET Q1 and lower N-MOSFET Q2 where shows in Figure11. The slew rate control is used to prevent the ringing of the VS node and the resistors also limited the peak current for sourcing or sinking the gate capacitance of external N-MOSFET.

11. PACKAGE DIMENSION

11.1 28-pin QFN (4mm*4mm)



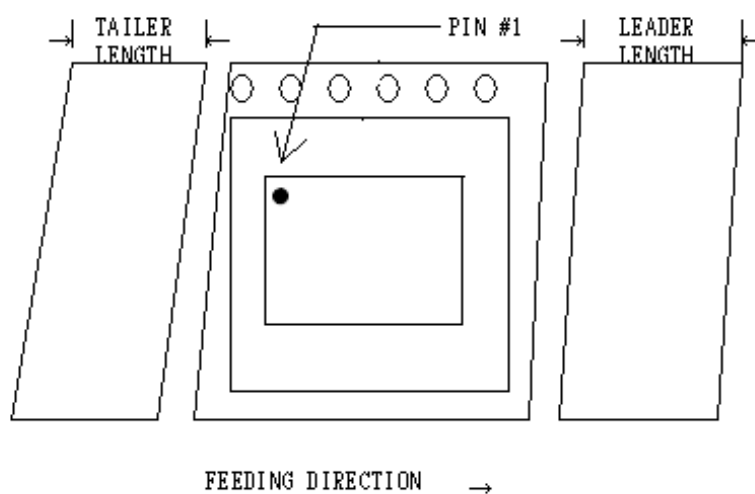
11.2 QFN 28L 4X4 MM² Land Pattern Design



Notes:

1. Unit : mm
2. The layout is just for reference.

11.3 Taping Specification



12. ORDERING INFORMATION

PART NUMBER	SUPPLIED AS	PACKAGE TYPE	OPERATION TEMPERATURE
NCT3612Y	4,000q'ty:	QFN28 Green Package	Commercial, -40°C to 105°C

12.1 Top Marking Specification



1st line: 05 – the part number NCT3612Y
 2nd line: Internal use only

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.01	2019/10/16	All	New.
0.02	2020/5/11	11,12	Modify the table in Chapter 6.3.

Important Notice

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